Wideband acquisition and SDR processing board

The board can be employed as a versatile test bed for a radar receiver or a SDR (Software Designed Radio) communication receiver; the high data rate of its ADC is suitable to process wideband signals or to implement sub-sampling techniques.

Technical data

ADC: ADS5400IPZP (12BIT, 1000 MSPS),

Core processing with a FPGA VIRTEX VI (6VSX315T) and a Power PC Freescale communicator (MPC8349).

Connection FPGA-external computer by a fast connection (Gbit Ethernet).

The FPGA comprises 5.090 Kb of RAM and 1.344 DSP48E1 units (each with 25x18 multipliers, an adder and an accumulator) and guarantees a massive computing power.

ADC clock Jitter and phase noise reduced by agile UHF synthesizer implemented by a UHF VCO (MC ROS-550PV), a pre-scaler, a PLL (ADF4112) and a low noise crystal reference generator.

All high frequency signal paths are implemented in a differential mode to minimize signal cross-talk and preserve integrity.