Wideband acquisition and SDR processing board

The board D00234-01A can be employed as a versatile test bed for a wideband radar receiver or a SDR (Software Defined Radio) communication receiver/waveform generator. The board can acquire I/Q baseband signal (implementing channel diversity) and generate the I/Q output baseband waveform.

Technical data

ADC		NOTE
Channel number	4 (2 in-phase, 2 in - quadrature)	Simultaneous sampling for each I/Q channel couple
Resolution	14 Bit	
Max sampling frequency	400 MHz	
Min input signal level for max dynamic	-10 dBm	Digital control gain(step: 1 db)
Max input level signal for max dynamic	0 dBm	
Input signal band	1280 MHz	(subsampling fashion)
SFDR (Spurious free dynamic range)	76 dB	
Input impedence	50 Ohm	
Input connectors	SMB	

DACs		NOTE
Channel number	2 (1 in-phase e 1-quadrature)	Simultaneous sampling
Resolution	14 Bit	
Max sampling frequency	400 MHz	
Output signal level	0 dBm	
SFDR (Spurios free dynamic range)	82 dB	
Output impedence	50 Ohm	
Output connectors	SMB	

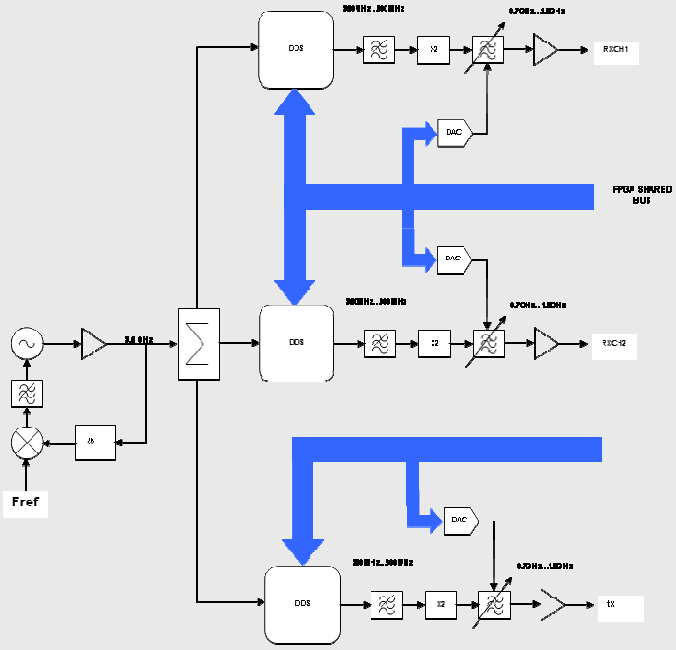
AUXILIARY DACs		NOTE
Auxiliary DAC number	5	
Resolution	12 Bit	
Output voltage range	0-5V / 0-15 V	Jumper selectable
Output connector	Multipin	

AUXILIARY ADCs		NOTE
Auxiliary DAC number	2	
Resolution	12 Bit	
Input voltage range	0-5 V	
Input connector	Multipin	

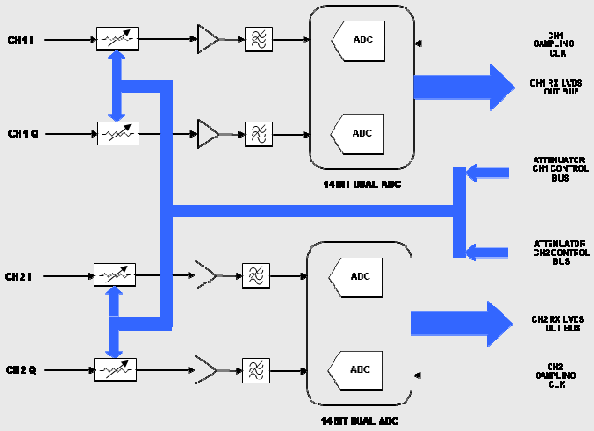
DDS		NOTE
Number of independent DDS	3	
Frequency range	10MHz-2.5GHz	
Frequency resolution	<1 Hz	
SFDR	<70 dBc	
Output level	0 dBm	
Output impedence	50 Ohm	
Connectors	SMB	

I/O		NOTE
Number of RS422 interfaces	4	Multipin connector
Number of RS232 interfaces	2	Multipin connector
Discrete digital signal number	32/16	Configurable
Number of LAN interfaces	2	100 Mb LAN, Multipin connector
Auxiliary channels	I2C e RS232 (level LVTTL)	I2C for IMU and RS232 for GPS

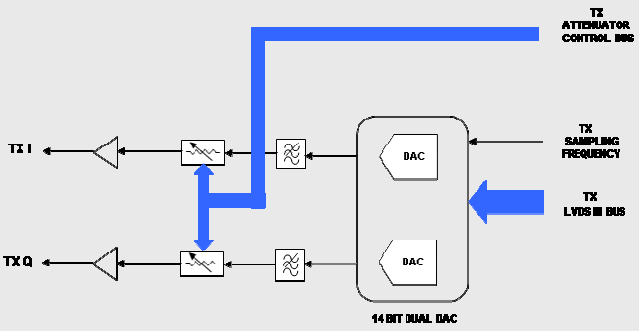
Miscellaneous		NOTE
Power source voltage	5V	
Absorbed power	<20W	
BOOT	On FLASH	Through LAN
Ventilation	Forced air /direction	Depends on assembling
Dimensions	250 x 200 mm	



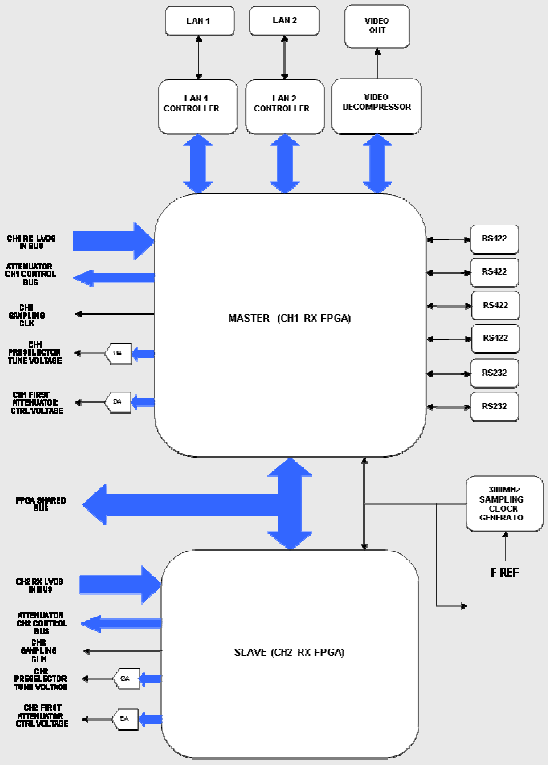
RF turning, based on DDS



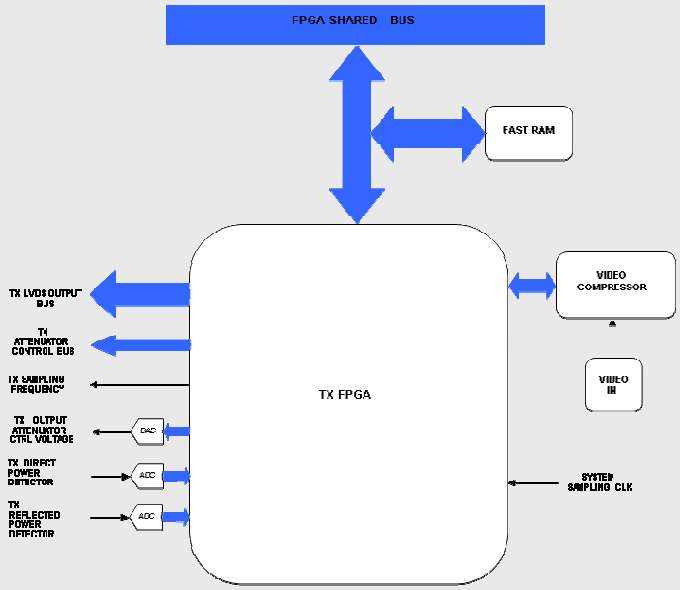
Analog to digital conversion section



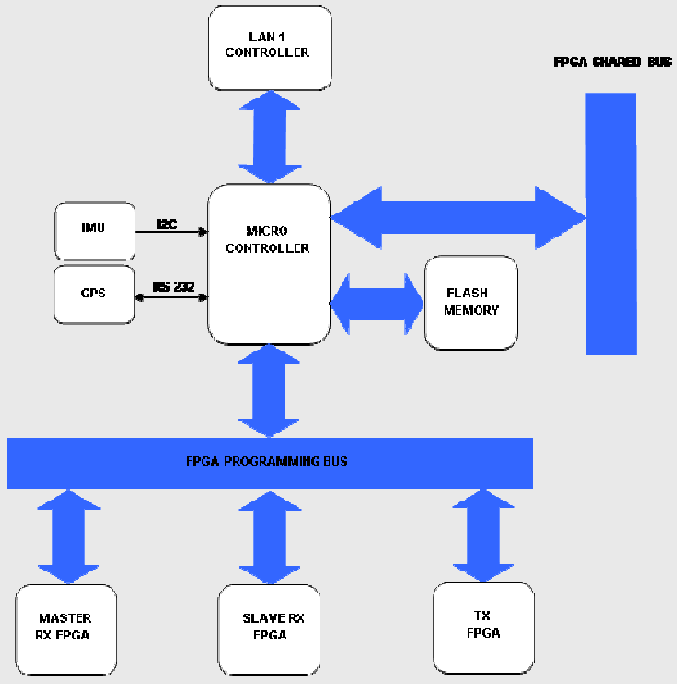
Digital to analog conversion section



Riceiver section based on two FPGA



Transmitter section based on a FPGA



Control section of FPGA including the firmware loading

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